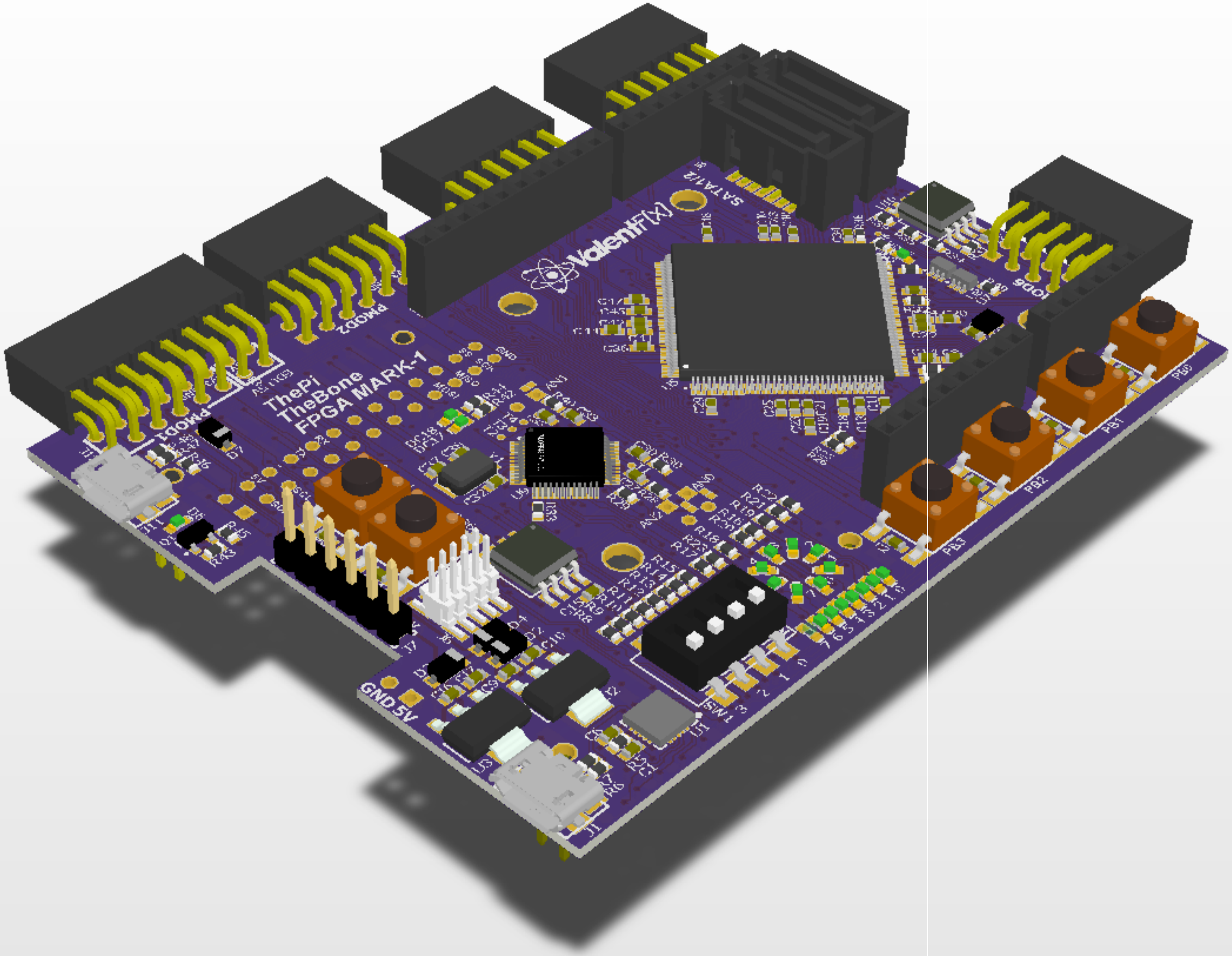
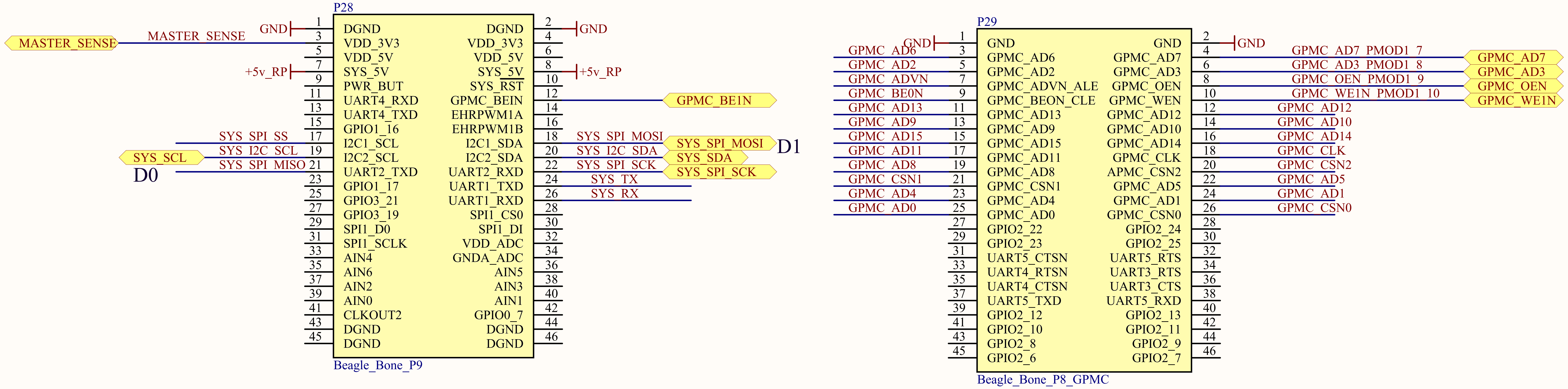
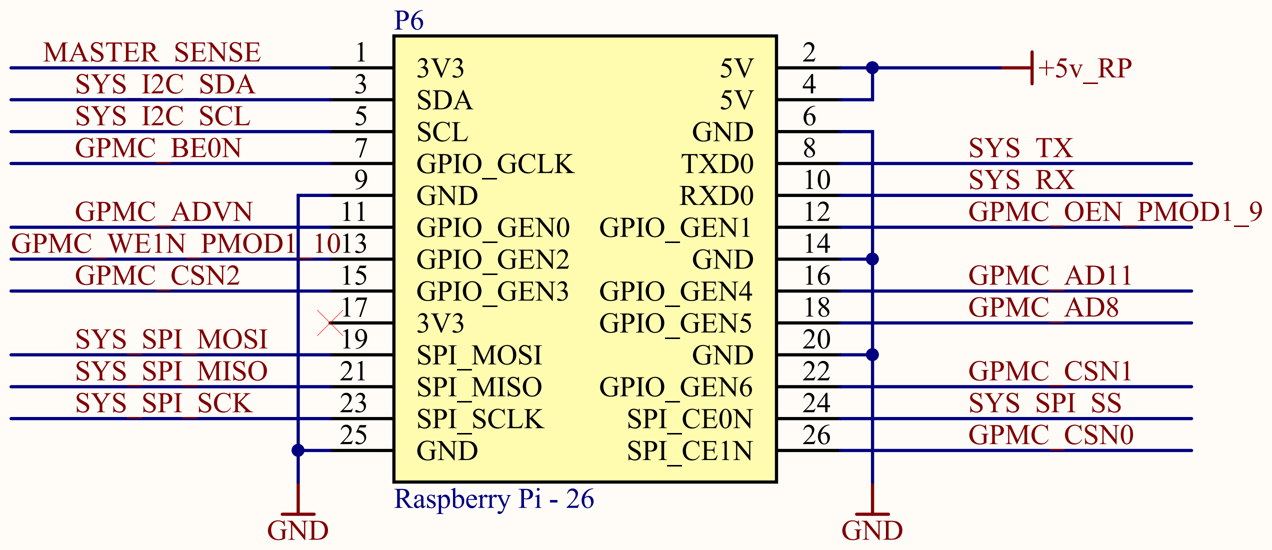

ValentF(x)
ThePi
TheBone
FPGA MARK-1
PMOD1
PMOD2
PMOD3
SATA1/2
PB0
PB1
PB2
PB3
SW1
GND 5V
J1
J6
J7

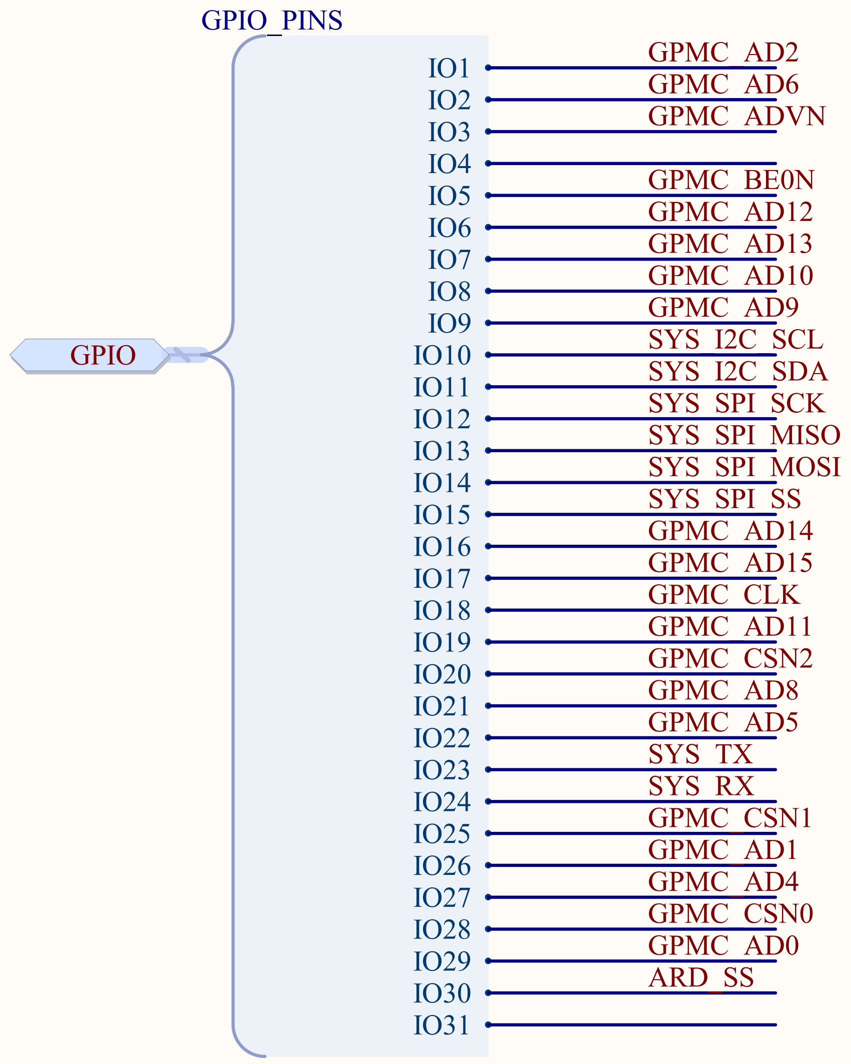
Beaglebone Headers



Raspberry Pi Header

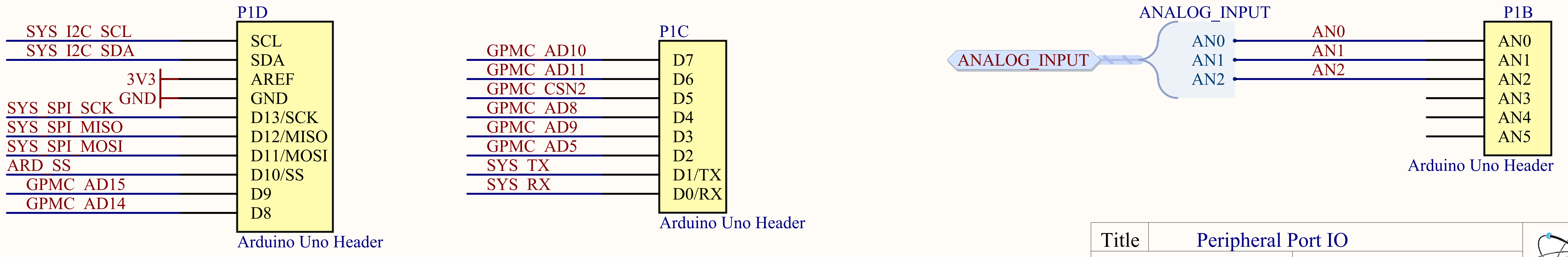


Raspberry Pi Header: The header allows for direct connection and powering from the Raspberry Pi. The header is stackable so that more RP Shields can be stacked on top. Optionally Arduino shields and PMODs can be used for further expansion and adding more functionality to RP



Arduino Header

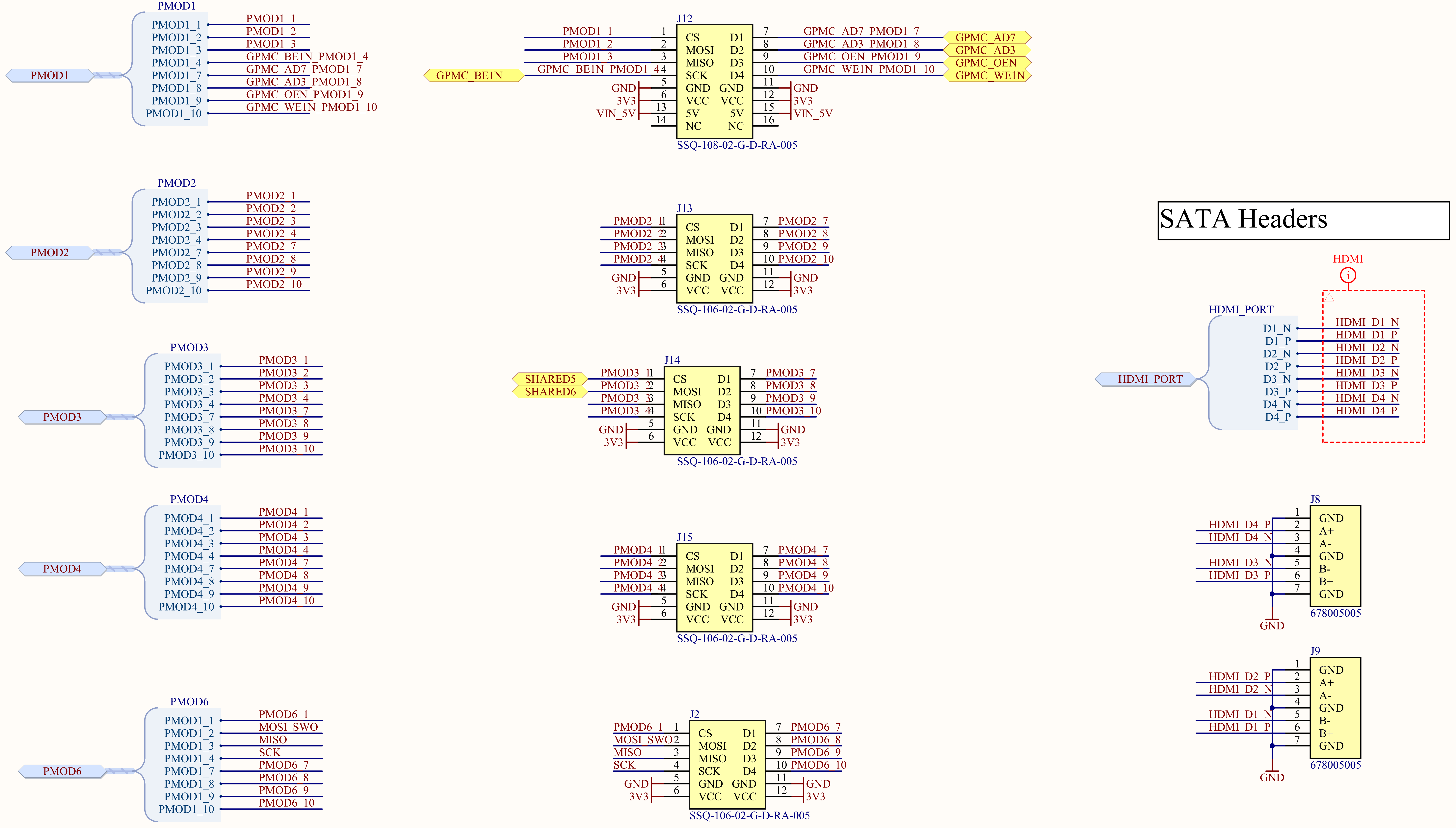
Arduino will have seperate CS



Title	Peripheral Port IO		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones

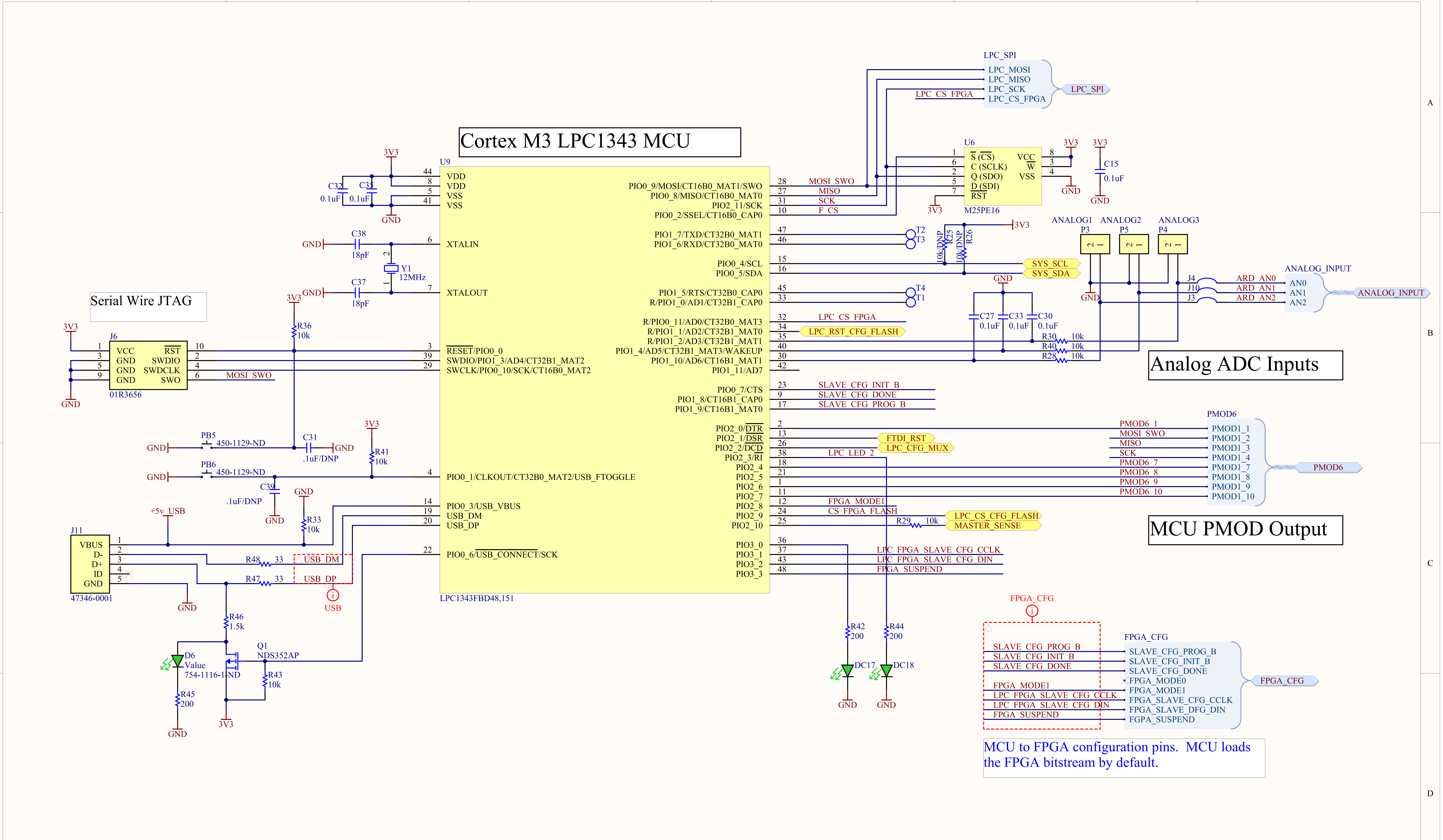
Digilent PMOD Headers

SATA Headers



Title	PMOD Expansion IO		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones

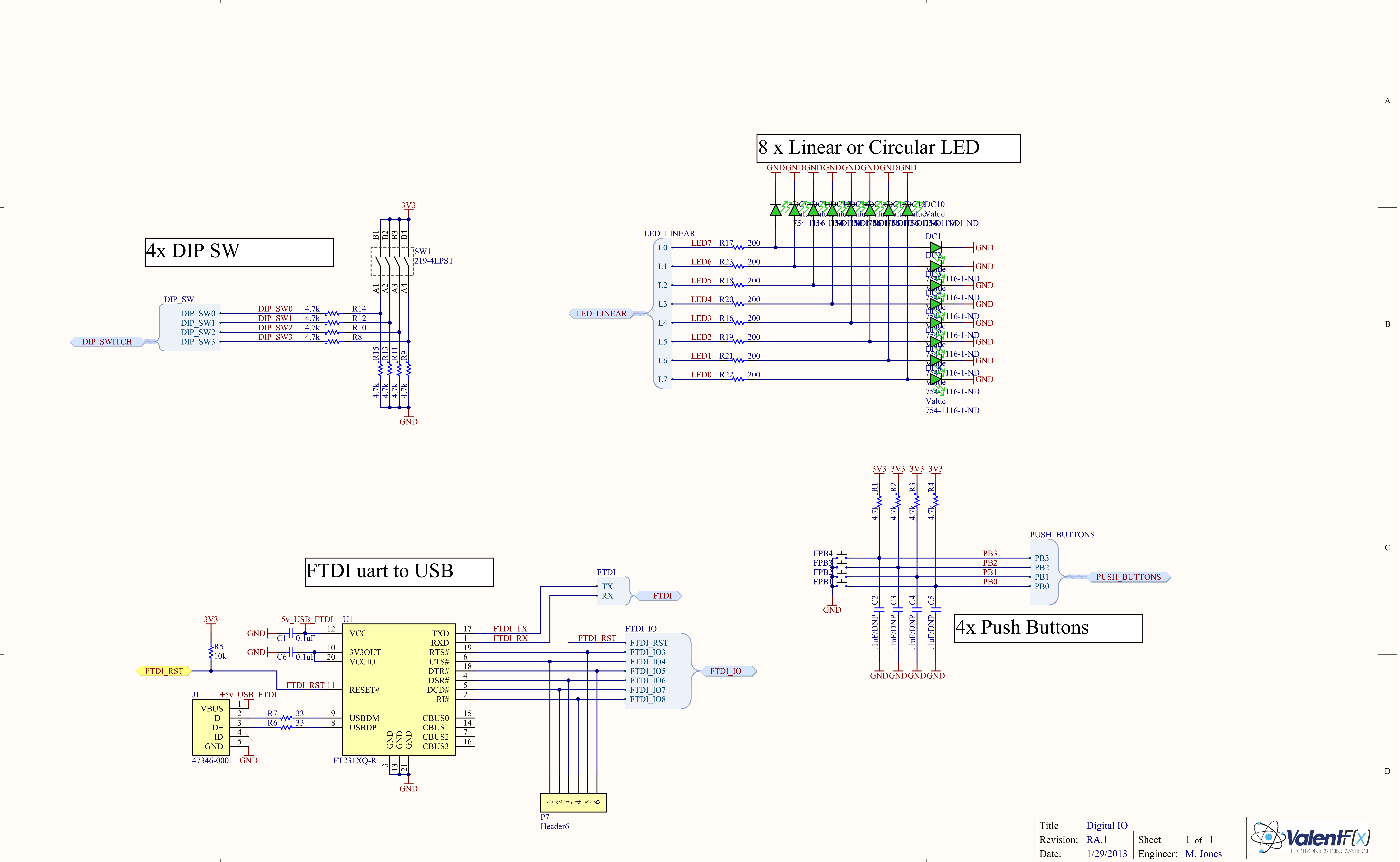
ValentF(x) ELECTRONICS INNOVATION



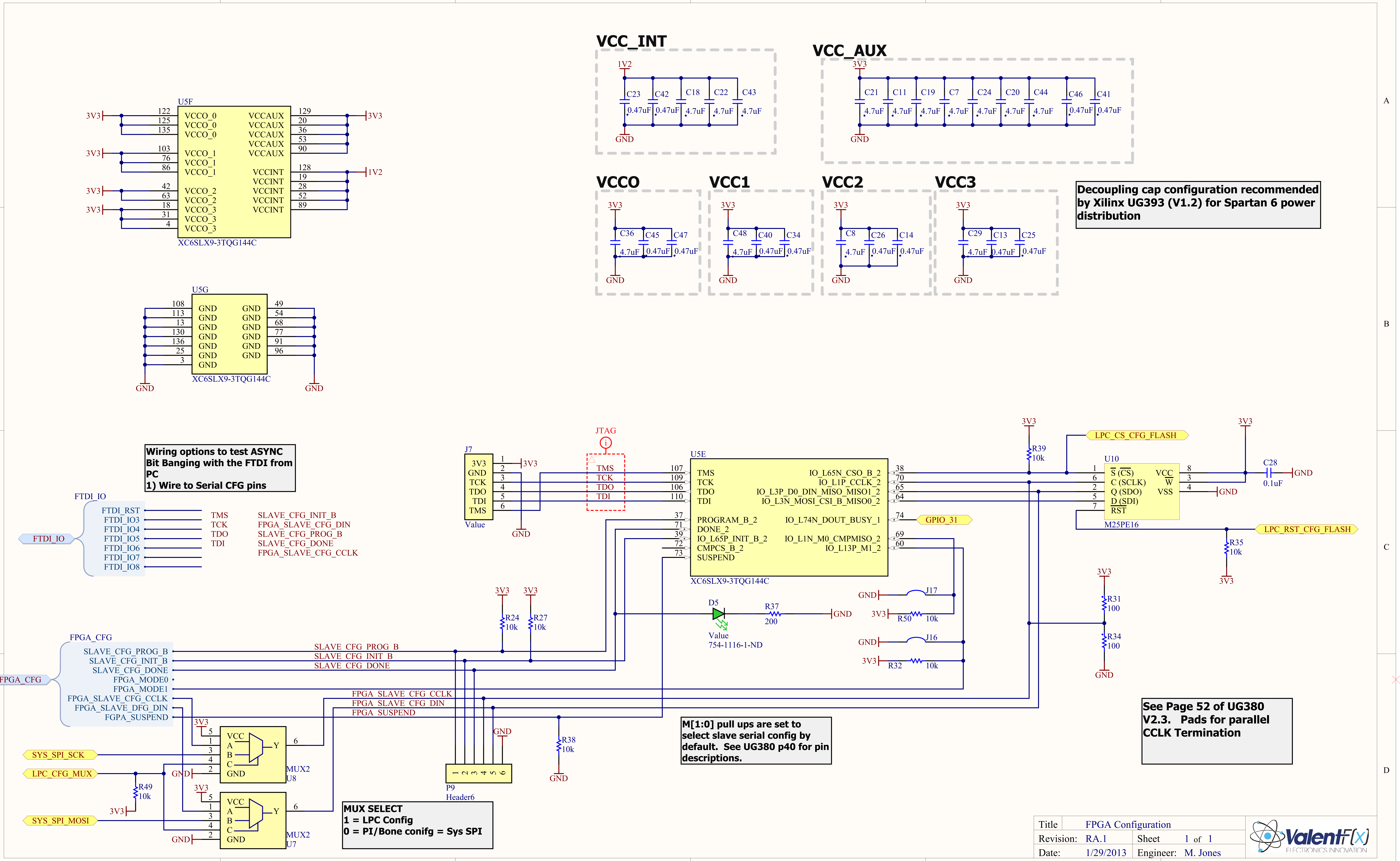
MCU to FPGA configuration pins. MCU loads the FPGA bitstream by default.

Title	MCU Logic		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones

ValentF(x) ELECTRONICS INNOVATION



Title	Digital IO		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones



Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution

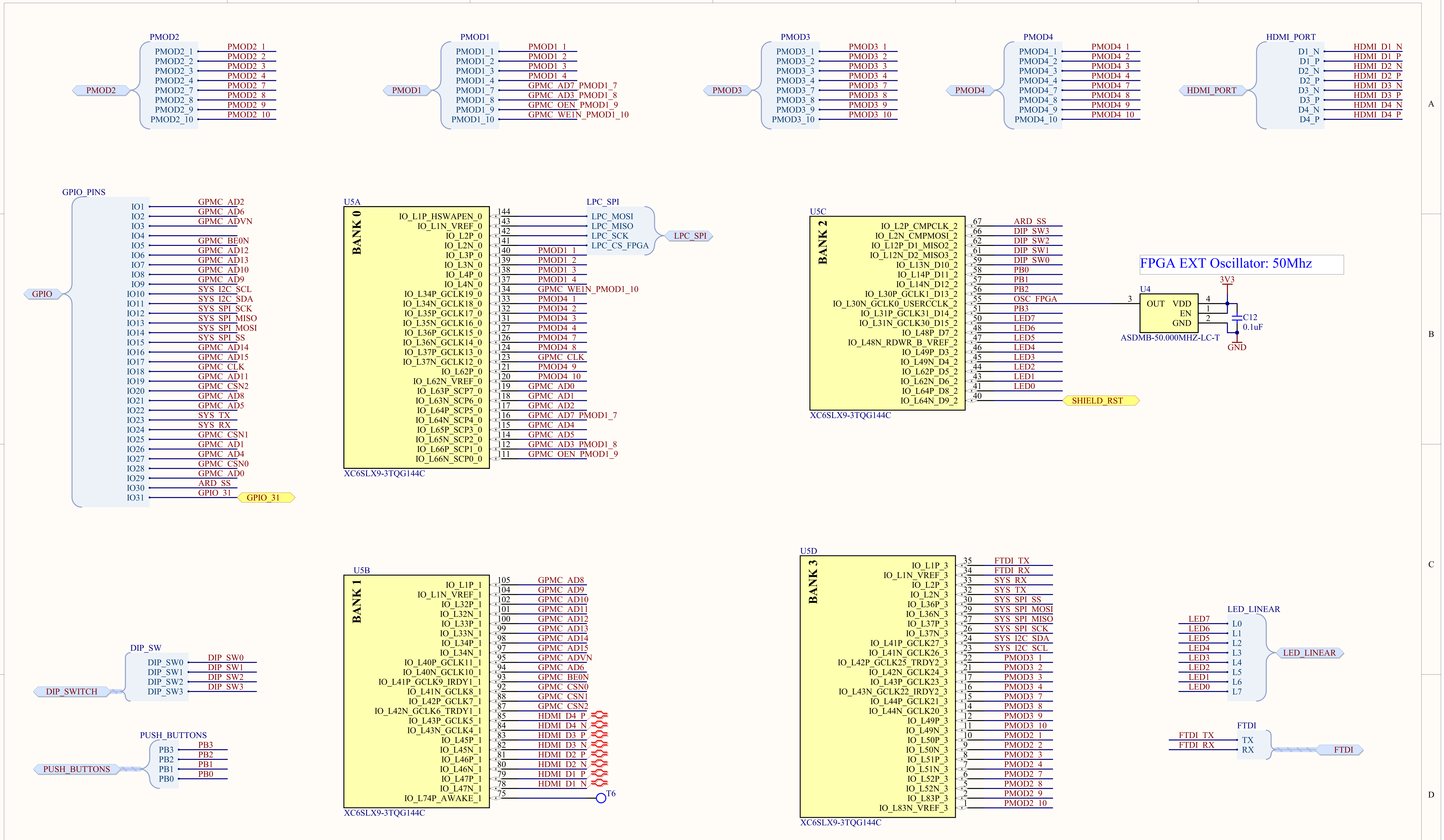
Wiring options to test ASYNC Bit Banging with the FTDI from PC
1) Wire to Serial CFG pins

M[1:0] pull ups are set to select slave serial config by default. See UG380 p40 for pin descriptions.

MUX SELECT
1 = LPC Config
0 = PI/Bone conifg = Sys SPI

See Page 52 of UG380 V2.3. Pads for parallel CCLK Termination

Title	FPGA Configuration		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones

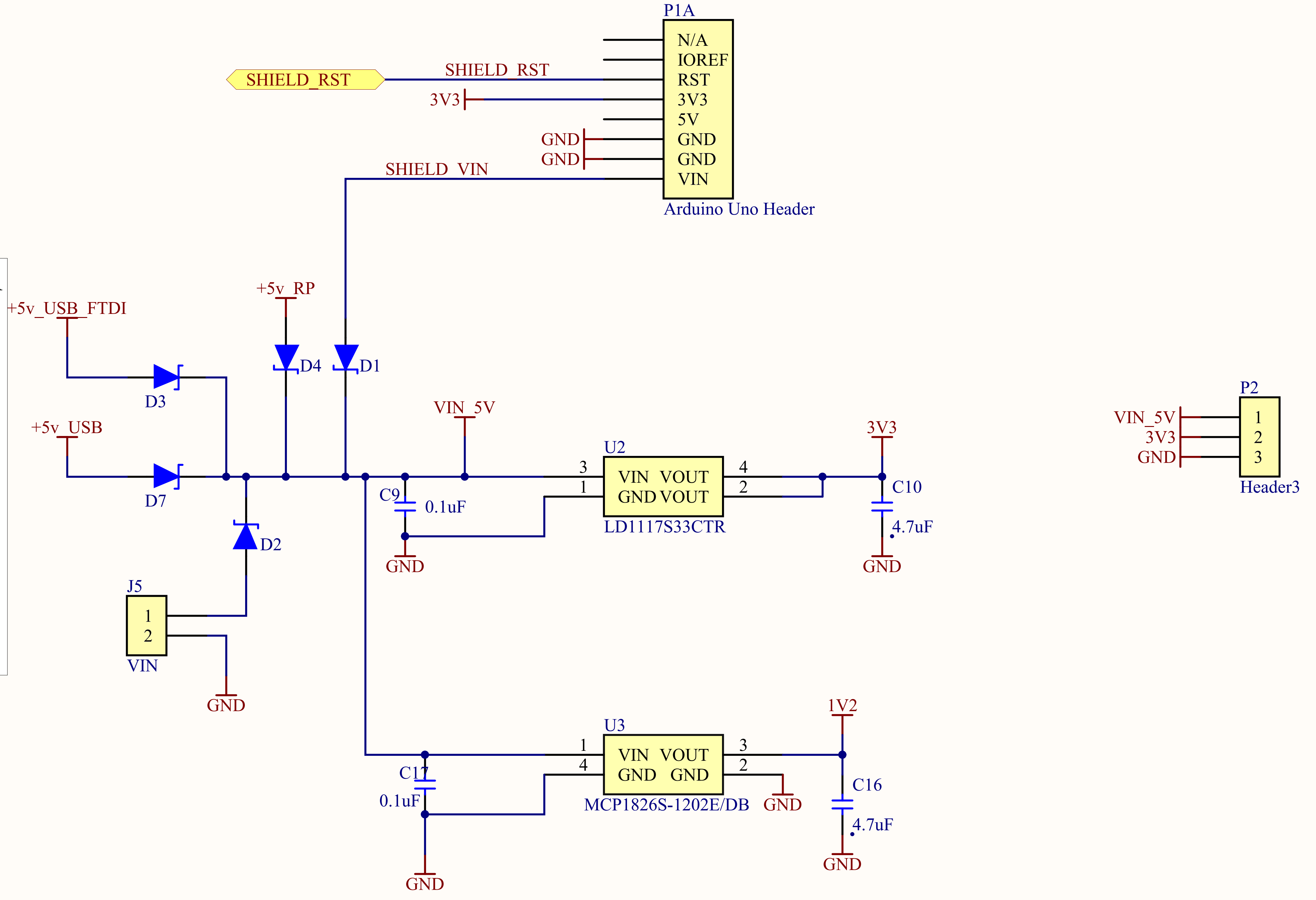


Title	FPGA Logic		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones

ValentF(x)
ELECTRONICS INNOVATION

Power: The LOGi-MARK-1 can be powered from a number of external sources including:

1.) Power Terminal (screw terminal) Not populated by default to reduce cost. (5V External Supply)
2.) MCU USB connector (5V Supply)
3.) FTDI USB connector (5V Supply)
4.) Arduino Master device (5V Supply)
5.) Raspberry Pi (5V supply)



Logo1
Valent Logo 1000

Logo2
Valent Logo 750

Title	Power Supply		
Revision:	RA.1	Sheet	1 of 1
Date:	1/29/2013	Engineer:	M. Jones

ELECTRONICS INNOVATION