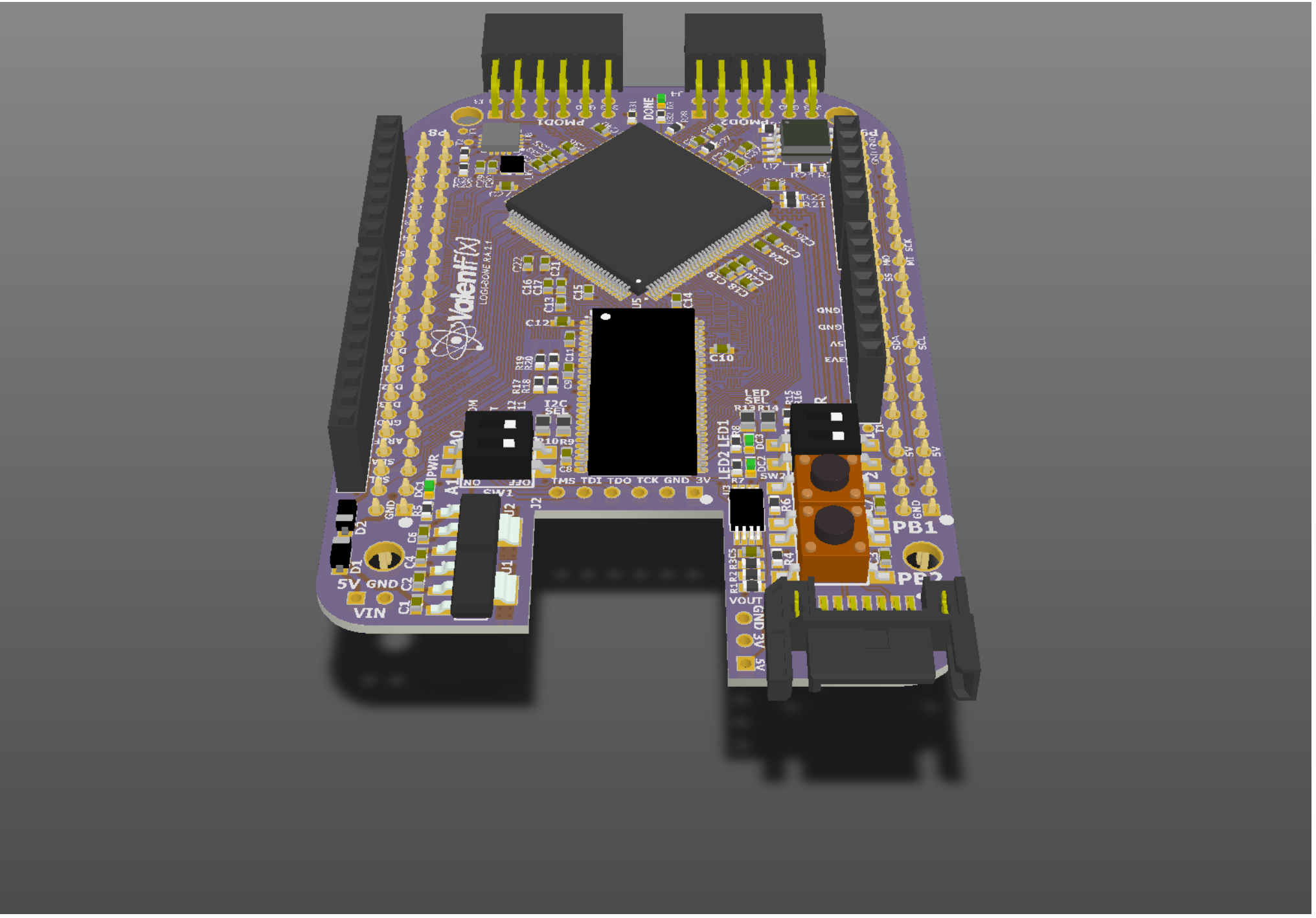
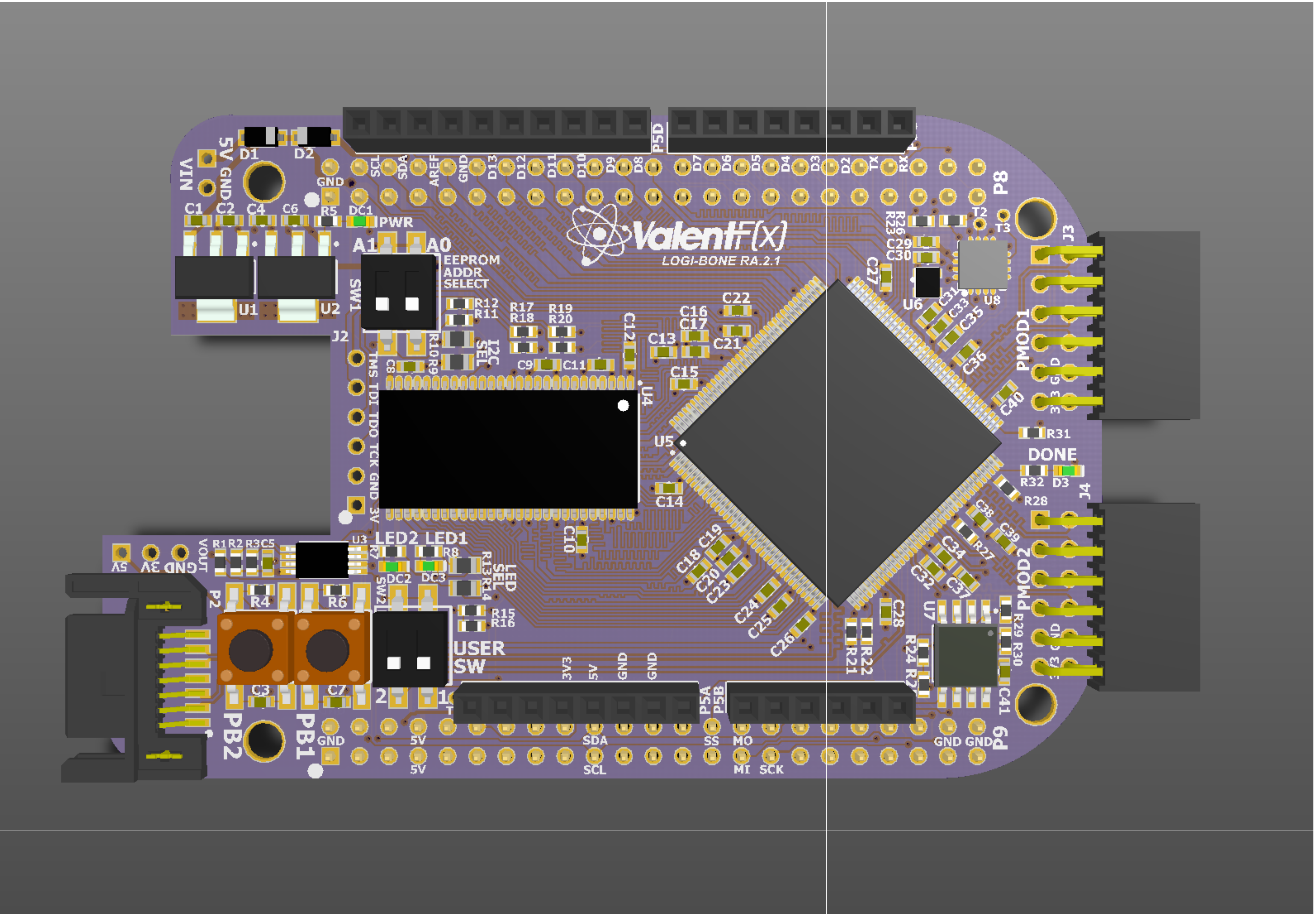
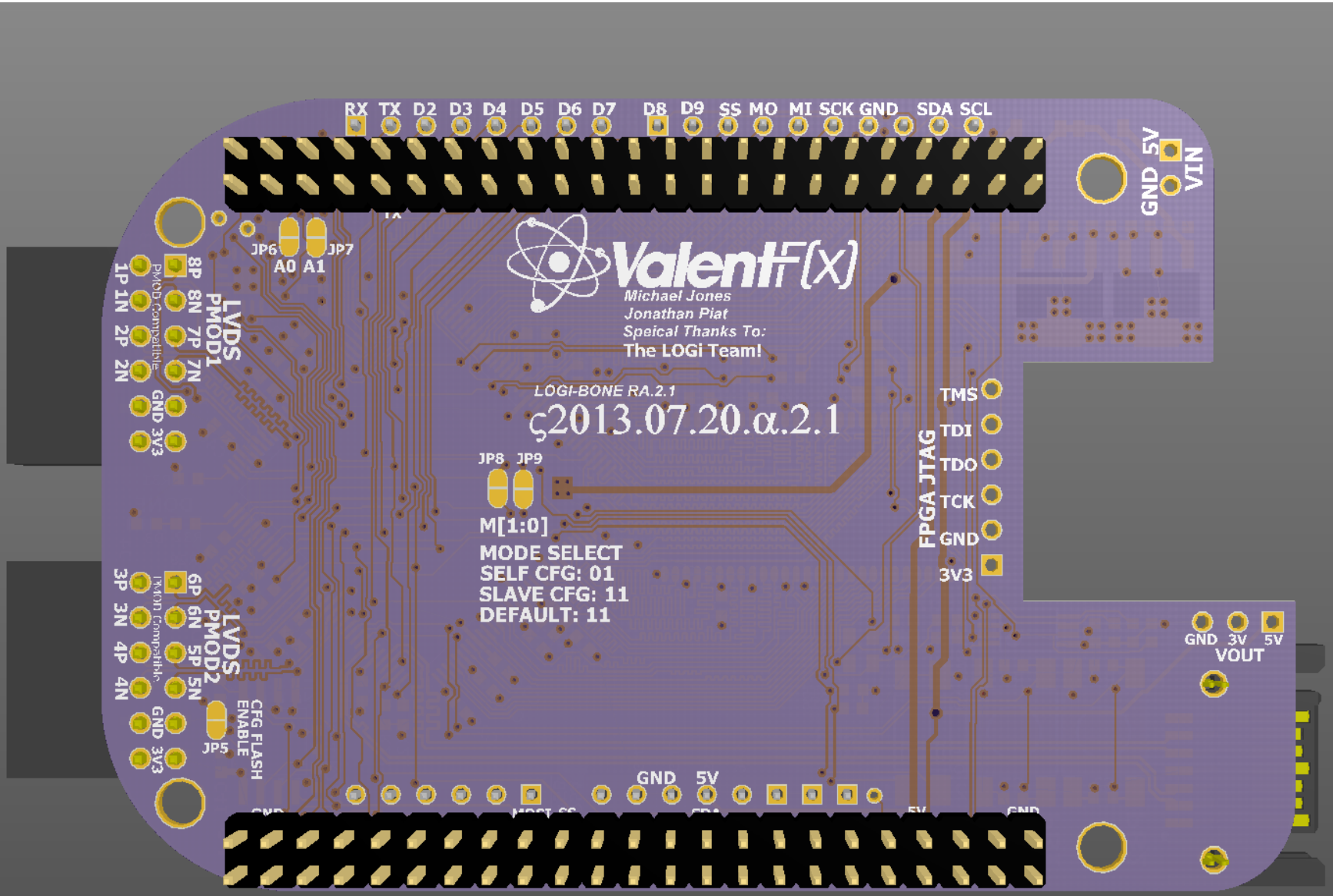

PMOD1
PMOD2
DONE
LOGI-BONE RA 2.1
LED SEL
I2C SEL
LED1
LED2
PWR
ON
OFF
SW1
SW2
PB1
PB2
TMS TDI TDO TCK GND 3V
5V GND
VIN
VOUT
GND
3V
5V
SDA
SCL
SCK
MO
SS

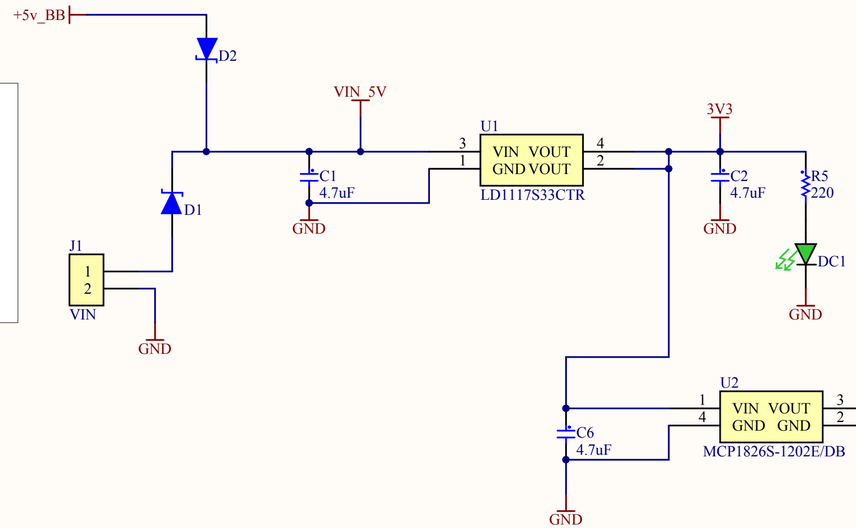


ValentF(x)
LOGI-BONE RA.2.1
P8
P9
PMOD1
PMOD2
EEPROM
ADDR
SELECT
A1
A0
SW1
PWR
DONE
USER
SW
PB1
PB2
LED2
LED1
LED
SEL
I2C
SEL
U1
U2
U3
U4
U5
U6
U7
U8
J2
J3
J4
D1
D2
D3
T2
T3
VIN
5V
GND
3V
VOUT
TMS
TDI
TDO
TCK
SCL
SDA
AREF
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
TX
RX
P5D
P5A
P5B
3V3
SS
MO
MI
SCK

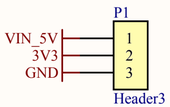

RX TX D2 D3 D4 D5 D6 D7 D8 D9 SS MO MI SCK GND SDA SCL
GND 5V VIN
JP6 JP7
A0 A1
ValentF(x)
Michael Jones
Jonathan Piat
Speical Thanks To:
The LOGi Team!
LOGI-BONE RA.2.1
ς2013.07.20.α.2.1
1P 1N 2P 2N GND 3V3
8P 8N 7P 7N
LVDS PMOD1
PMOD Compatible
JP8 JP9
M[1:0]
MODE SELECT
SELF CFG: 01
SLAVE CFG: 11
DEFAULT: 11
TMS
TDI
TDO
TCK
GND
3V3
FPGA JTAG
3P 3N 4P 4N GND 3V3
6P 6N 5P 5N
LVDS PMOD2
PMOD Compatible
JP5
CFG FLASH ENABLE
GND 5V
GND 3V 5V
VOUT

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header J1.



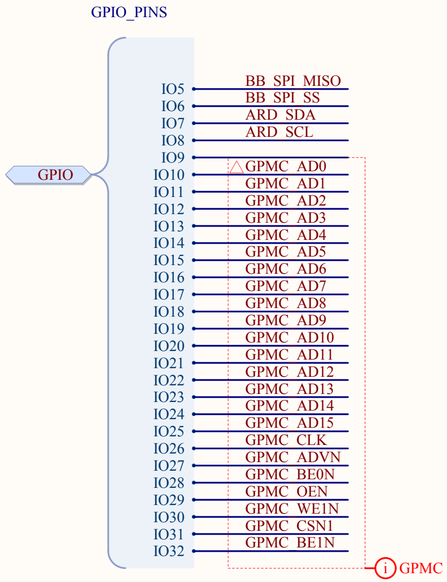
1 x Auxillary Power output Headers

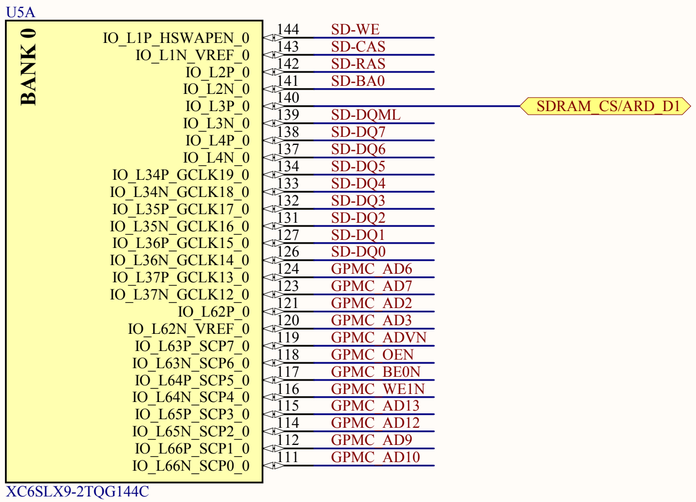


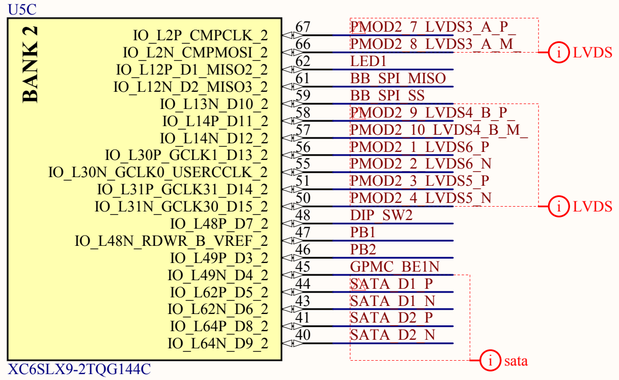
Logo1
Valent Logo 750
Logo2
Valent Logo 1000

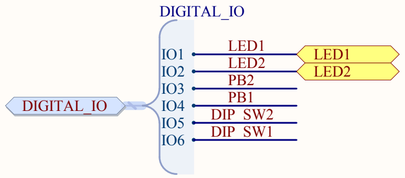
Title	Power Supply		
Revision:	RA2.1	Sheet	1 of 6
Date:	9/10/2013	Engineer:	MJones

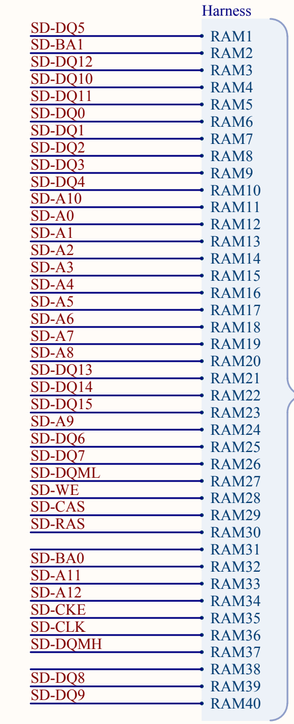
ValentF(X) ELECTRONICS INNOVATION

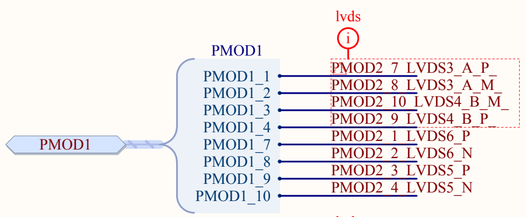


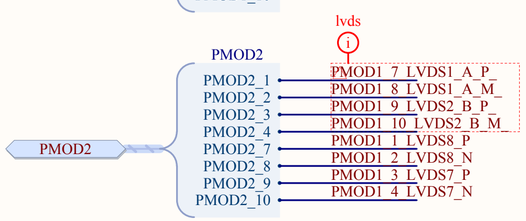


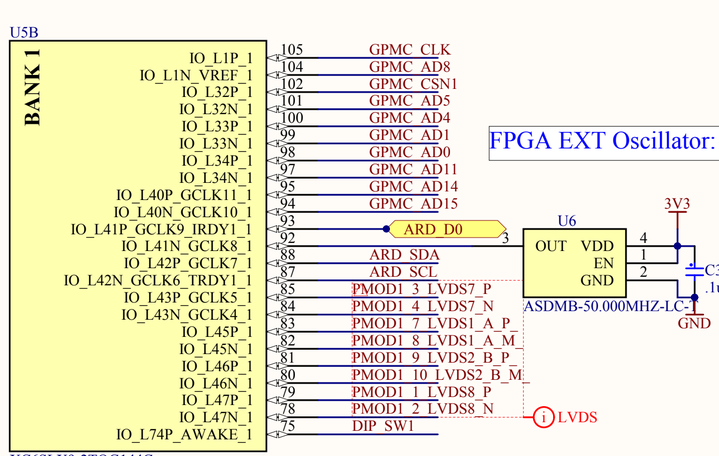




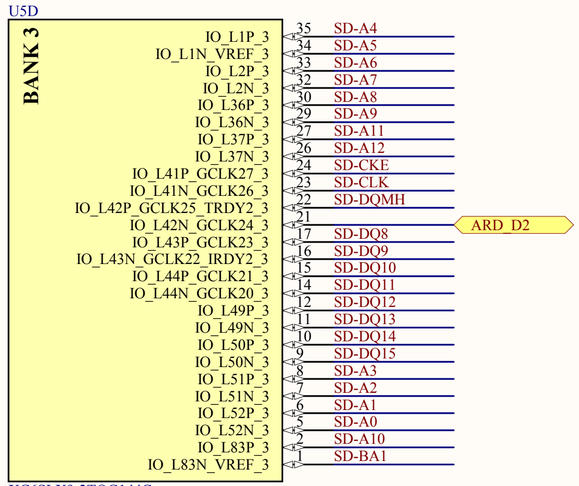






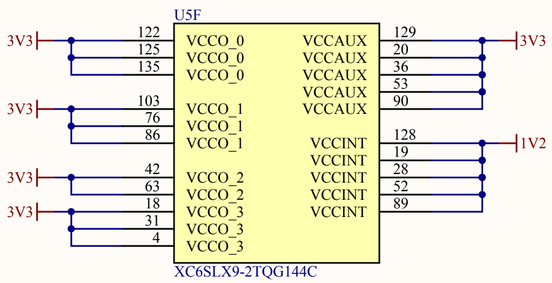


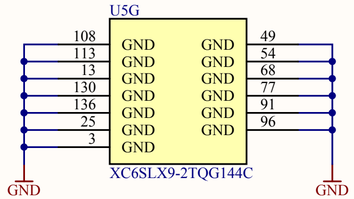
FPGA EXT Oscillator: 50Mhz

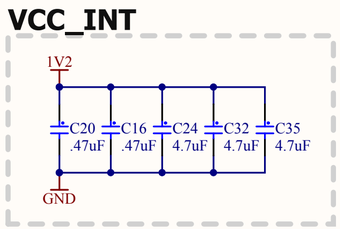


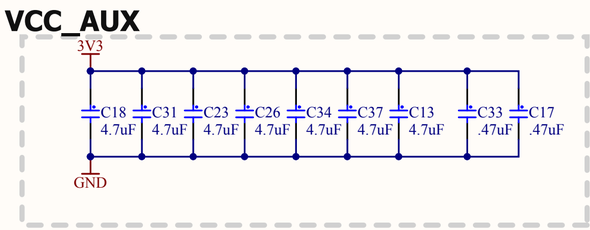
Title	FPGA Logic		
Revision:	RA2.1	Sheet	2 of 6
Date:	9/10/2013	Engineer:	MJones

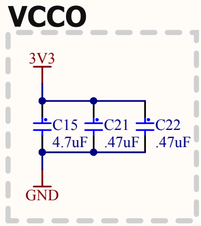
ValentF(x) ELECTRONICS INNOVATION

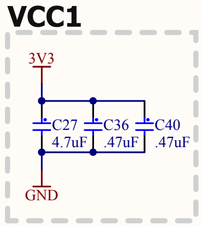


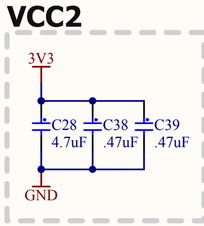


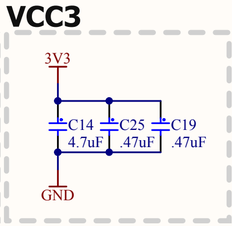




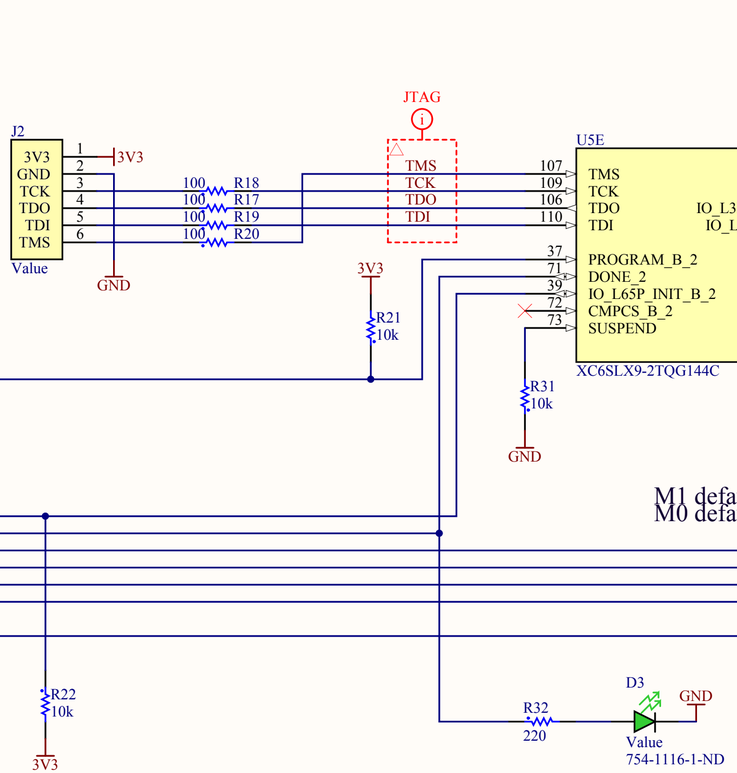








Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution



CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA

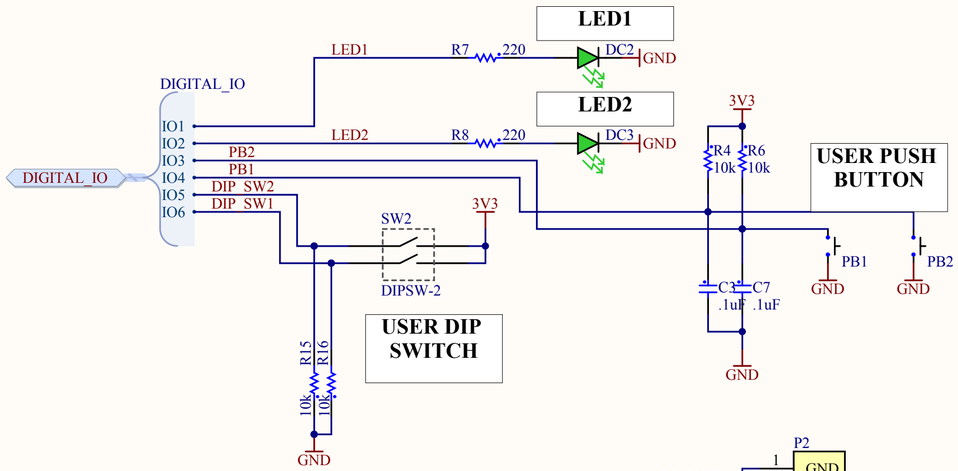
M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig

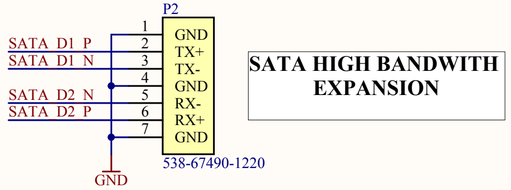
See Page 52 of UG380 V2.3. Pads for parallel CCLK Termination

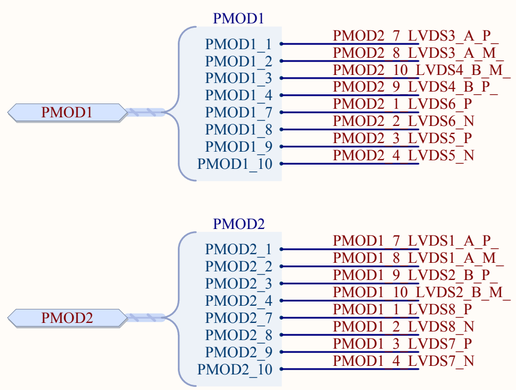
Title	FPGA Configuration		
Revision:	RA2.1	Sheet	3 of 6
Date:	9/10/2013	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

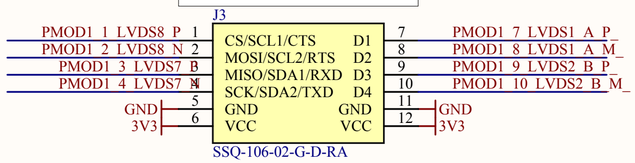
FPGA Digital IO



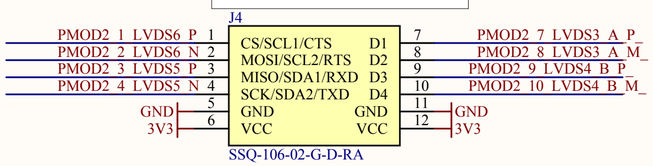




PMOD1 PORT

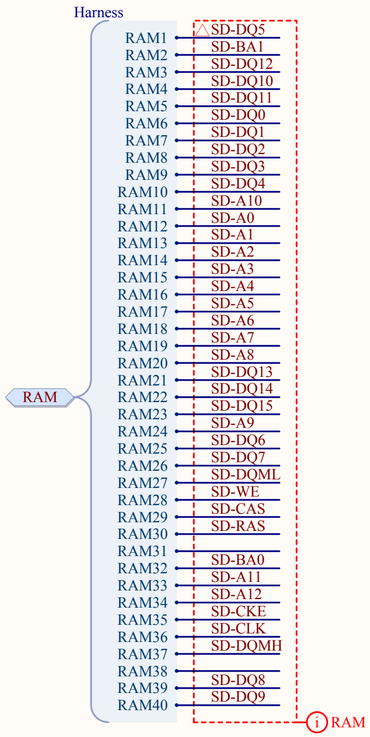


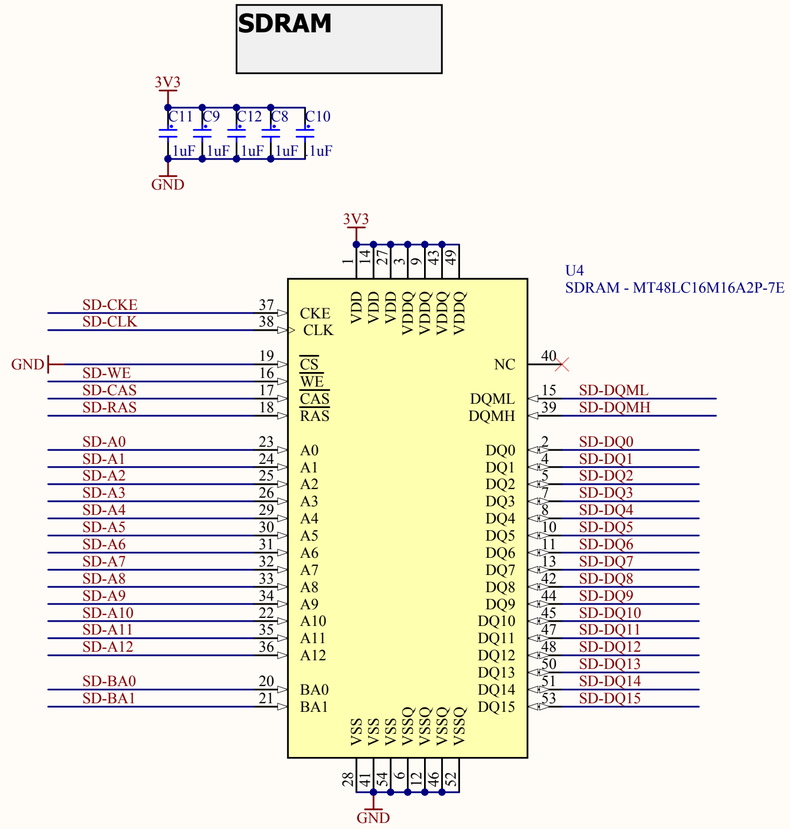
PMOD2 PORT



Title	Digital IO		
Revision:	RA2.1	Sheet	4 of 6
Date:	9/10/2013	Engineer:	MJones

ValentF(x) ELECTRONICS INNOVATION

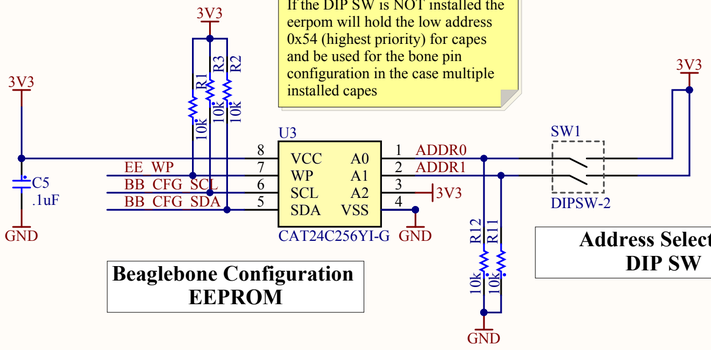




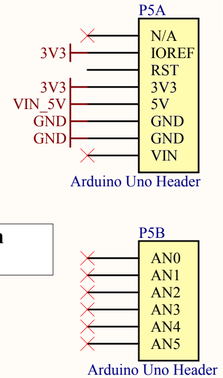
Title	RAM		
Revision:	RA2.1	Sheet	5 of 6
Date:	9/10/2013	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION

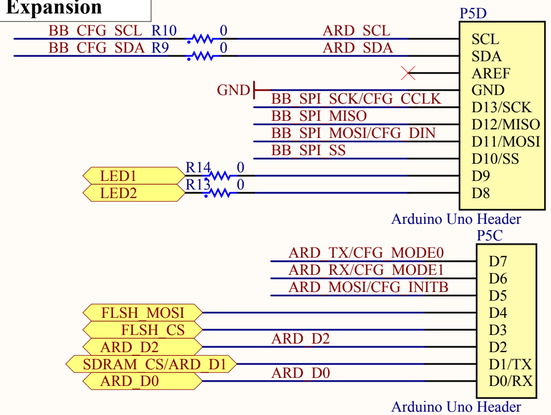
Beaglebone Configuration EEPROM



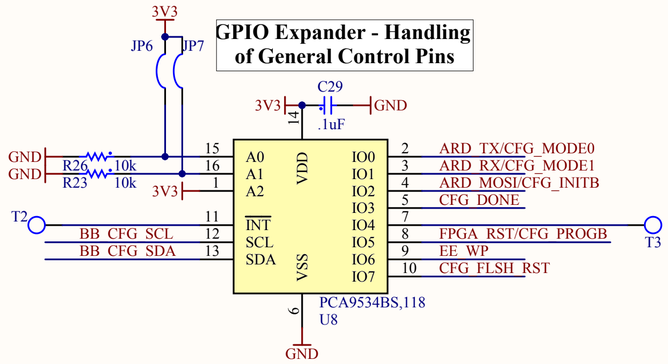
Address Selection DIP SW



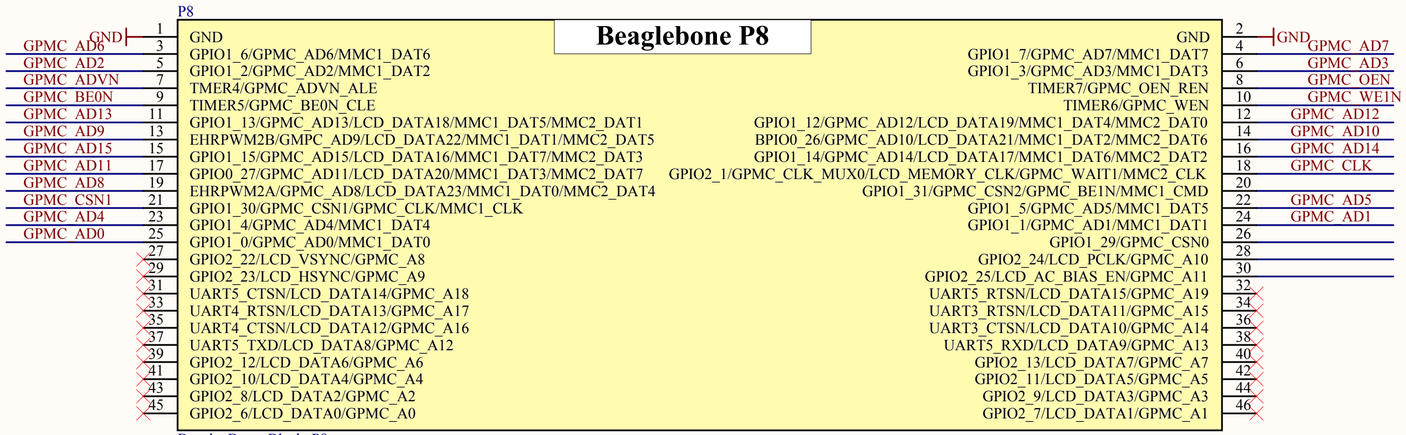
Arduino Header - Arduino Shield Expansion



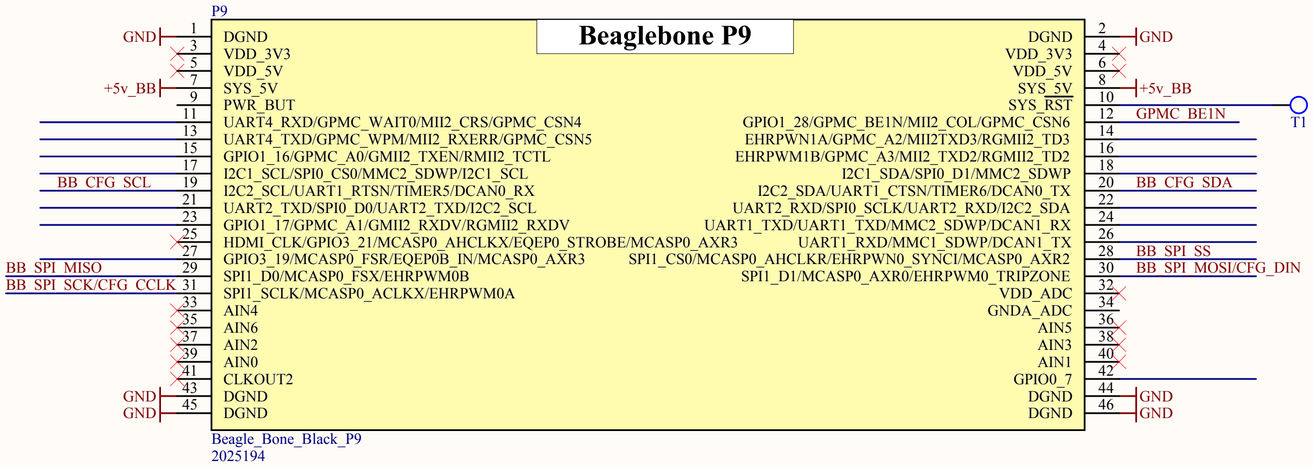
GPIO Expander - Handling of General Control Pins

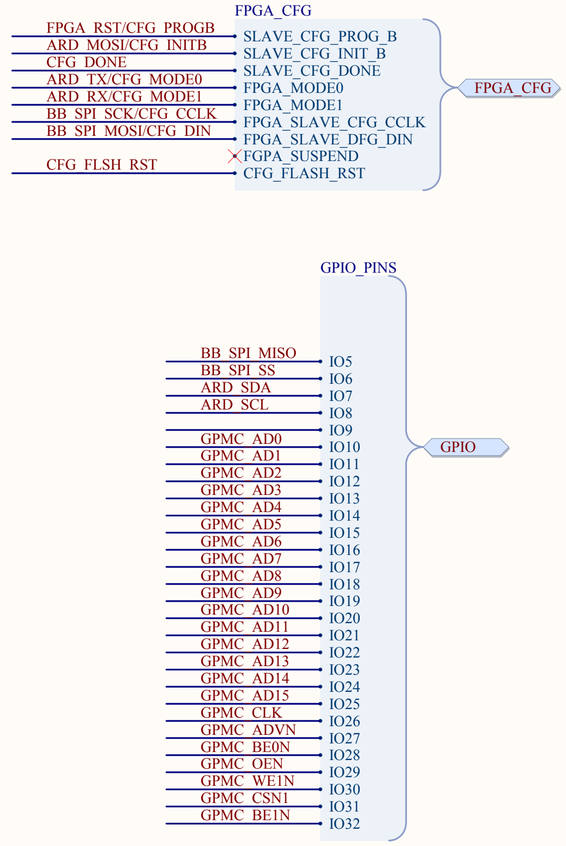


Beaglebone P8



Beaglebone P9





Title	Peripheral Port IO		
Revision:	RA2.1	Sheet	6 of 6
Date:	9/10/2013	Engineer:	MJones

ValentF(X) ELECTRONICS INNOVATION